

## **FUNCTIONAL TEST DESIGN FOR TESTABILITY (DFT) AND TEST ARCHITECTURE FOR DECREASED TESTER CHANNEL RESOURCES**

### **ABSTRACT**

According to one aspect of the present invention, multiple pins of a chip are  
5 connected to a single test channel of a tester. This allows an older tester with fewer  
test channels to be used with newer chips that have more pins than there are test  
channels.